Attorney: Jun-Young E. Jeon
Docket No.: 51708/JEJ/B600
Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
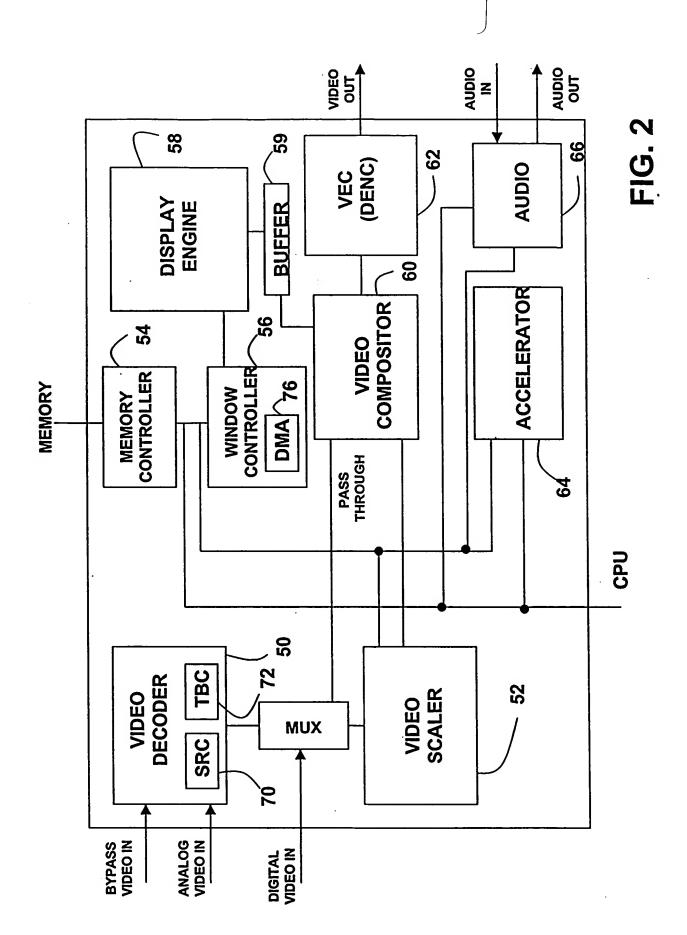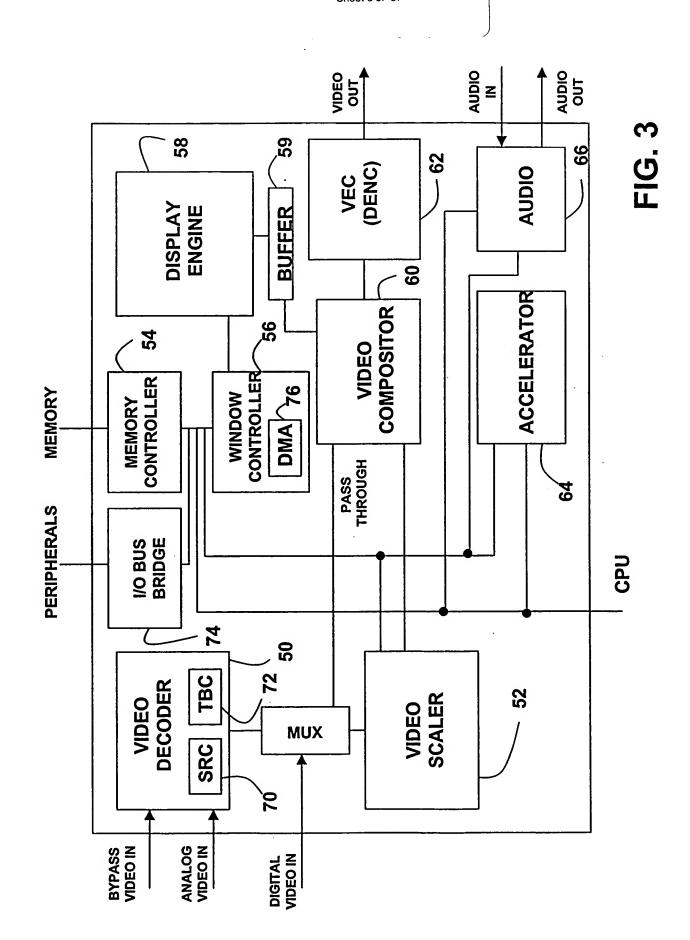Memory Architecture
                    Sheet 1 of 37

FIG. 1

A..orney. Jun-Young E. Jeon
Docket No.: 51708/JEJ/B600
Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
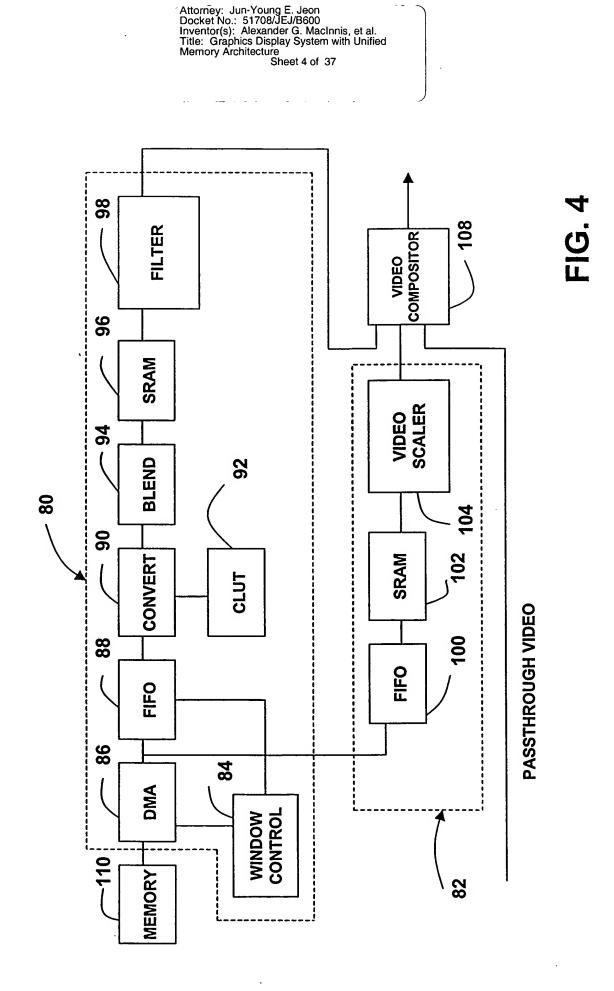Memory Architecture
Sheet 2 of 37

FIG. 2

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Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
Memory Architecture
Sheet 3 of 37

VIDEO OUT

AUDIO IN

AUDIO OUT

DISPLAY ENGINE 58

BUFFER 59

VEC (DENC) 62

AUDIO 66

MEMORY

MEMORY CONTROLLER 54

WINDOW CONTROLLER 56

DMA 76

VIDEO COMPOSITOR 60

ACCELERATOR 64

PERIPHERALS

I/O BUS BRIDGE

PASS THROUGH

CPU

VIDEO DECODER 74

TBC 72

SRC 70

50

MUX

VIDEO SCALER 52

BYPASS VIDEO IN

ANALOG VIDEO IN

DIGITAL VIDEO IN

FIG. 3

Attorney: Jun-Young E. Jeon
Docket No.: 51708/JEJ/B600
Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
Memory Architecture
Sheet 4 of 37

FIG. 4

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Docket No.: 51708/JEJ/B600
Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
Memory Architecture
Sheet 5 of 37

FIG. 5

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Docket No.: 51708/JEJ/B600
Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
Memory Architecture
Sheet 6 of 37

FIG. 6

WINDOW OPERATION [31:30]

WORD 0

WIN FORMAT [29:26]	WINDOW MEMORY START [25:0]

WORD 1

WIN LAYER [31:28]	WINDOW MEMORY PITCH [27:16]	WINDOW COLOR [15:0]

ALPHA TYPE [31:30]

WORD 2

WINDOW ALPHA [29:22]	H D	WINDOW Y-END [20:11]	H D	WINDOW Y-START [9:0]

WINDOW FILTER ENABLE [26]

WORD 3

NOT USED [31:27]	BLANK START PIXEL [25:22]	H D	WINDOW X-SIZE [20:11]	H D	WINDOW X-START [9:0]

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Docket No.: 51708/JEJ/B600
Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
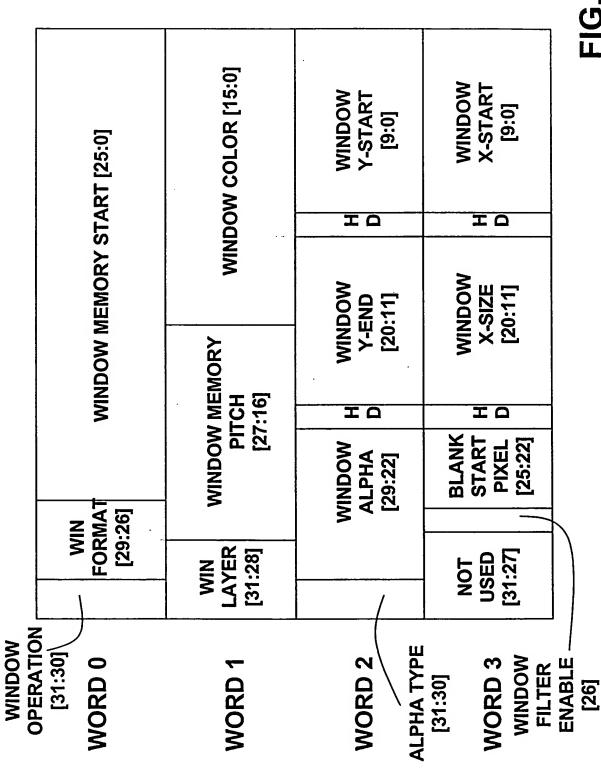Memory Architecture
Sheet 7 of 37

8 WINDOW DESCRIPTORS

WD PARAMETERS

SMALLEST WD
PARAMETERS

300h
300g
300f
300e
300d
300c
300b
300a

WDO

MUX

302

SORTING

304

SMALLEST WD
PARAMETERS

DMA
(ASSEMBLE
HEADER AND
REQUEST MEM-
ORY DATA)

306

WD HEADER,
GFX DATA

GFX
FIFO

308

WD HEADER,
GFX DATA

GFX DISP

MEMORY CONTROLLER

FIG.7

Attorney: Jun-Young E. Jeon
Docket No.: 51708/JEJ/B600
Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
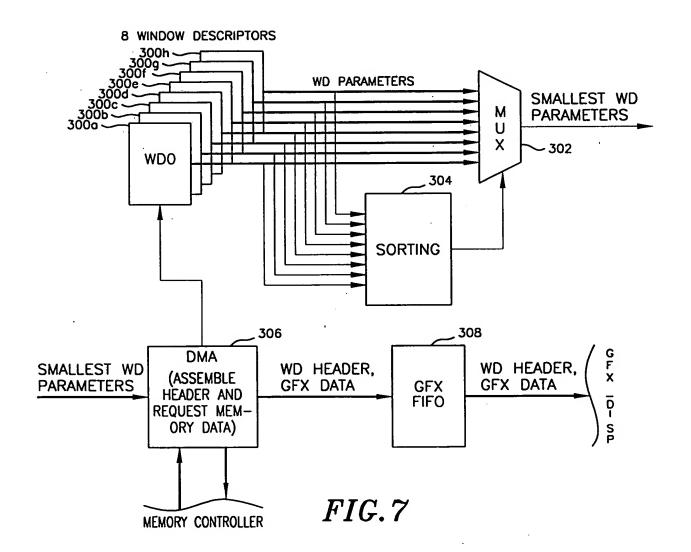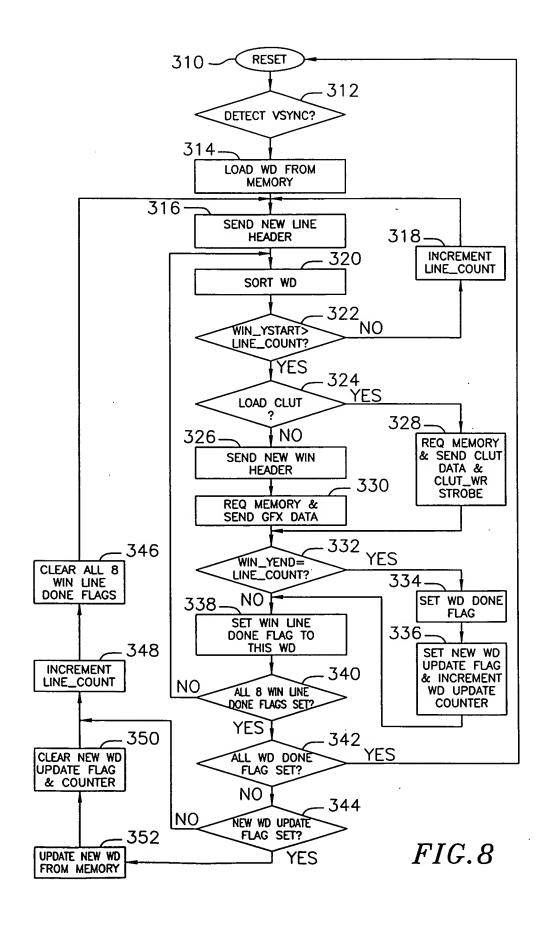Memory Architecture
Sheet 8 of 37

310 — RESET

312
DETECT VSYNC?

314 — LOAD WD FROM MEMORY

316 — SEND NEW LINE HEADER

318 — INCREMENT LINE_COUNT

320 — SORT WD

322 WIN_YSTART> LINE_COUNT? NO

YES

324 LOAD CLUT ? YES

326 — NO SEND NEW WIN HEADER

328 — REQ MEMORY & SEND CLUT DATA & CLUT_WR STROBE

330 — REQ MEMORY & SEND GFX DATA

332 WIN_YEND= LINE_COUNT? YES

334 — SET WD DONE FLAG

346 — CLEAR ALL 8 WIN LINE DONE FLAGS

338 — NO SET WIN LINE DONE FLAG TO THIS WD

336 — SET NEW WD UPDATE FLAG & INCREMENT WD UPDATE COUNTER

348 — INCREMENT LINE_COUNT

340 ALL 8 WIN LINE DONE FLAGS SET? NO

YES

350 — CLEAR NEW WD UPDATE FLAG & COUNTER

342 ALL WD DONE FLAG SET? YES

NO

352 — UPDATE NEW WD FROM MEMORY

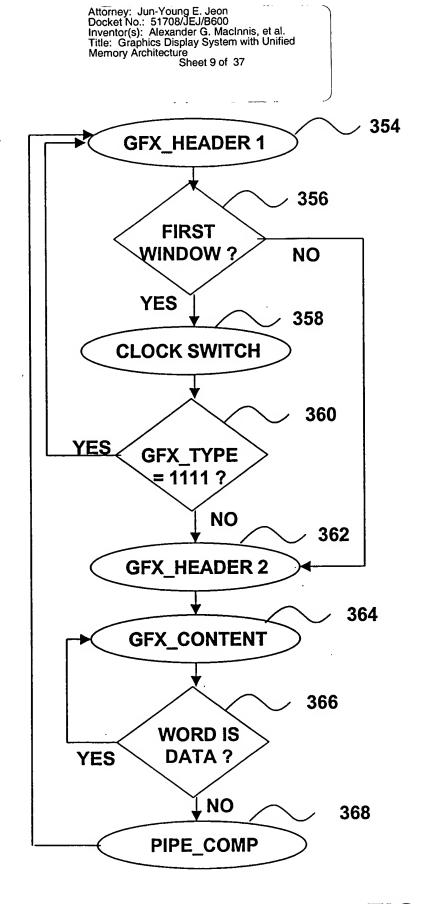344 NEW WD UPDATE FLAG SET? NO

YES

FIG.8

Attorney: Jun-Young E. Jeon
Docket No.: 51708/JEJ/B600
Inventor(s): Alexander G. MacInnis, et al.
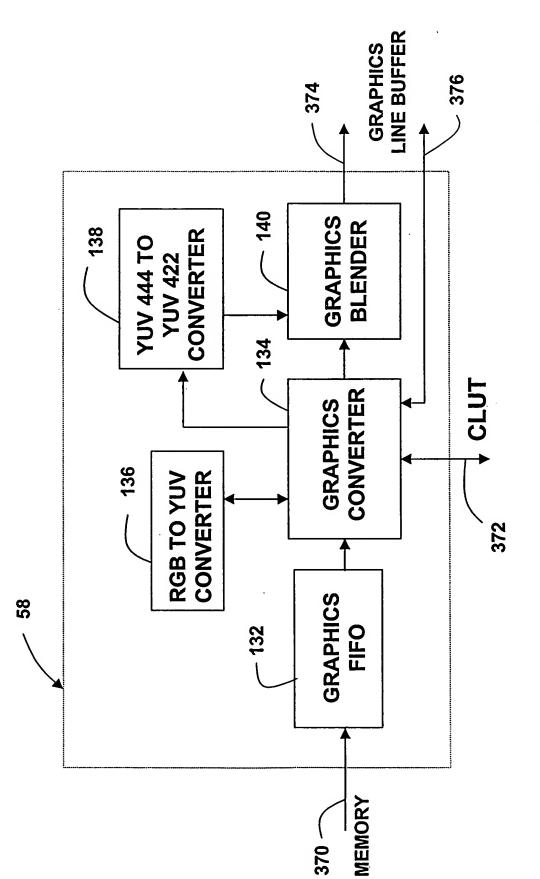Title: Graphics Display System with Unified
Memory Architecture
Sheet 9 of 37

GFX_HEADER 1 — 354

FIRST WINDOW ? — 356

NO

YES

CLOCK SWITCH — 358

GFX_TYPE = 1111 ? — 360

YES

NO

GFX_HEADER 2 — 362

GFX_CONTENT — 364

WORD IS DATA ? — 366

YES

NO

PIPE_COMP — 368

FIG. 9

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Docket No.: 51708/JEJ/B600
Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
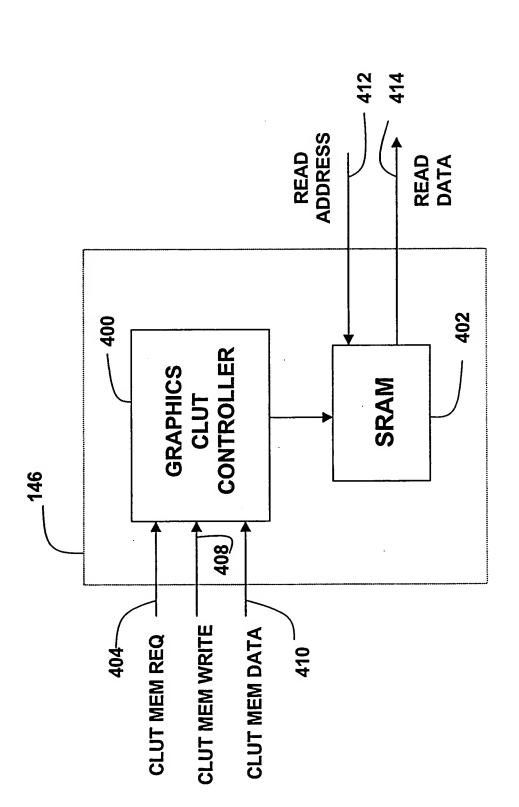Memory Architecture
Sheet 10 of 37

FIG. 10

Attorney: Jun-Young E. Jeon
Docket No.: 51708/JEJ/B600
Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
Memory Architecture
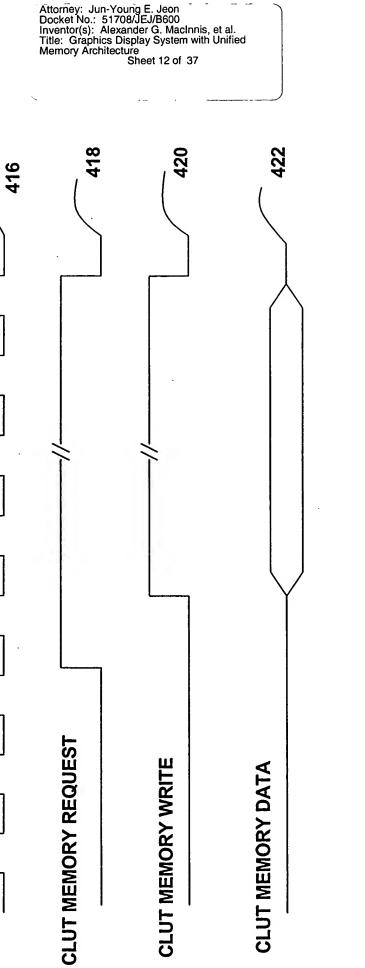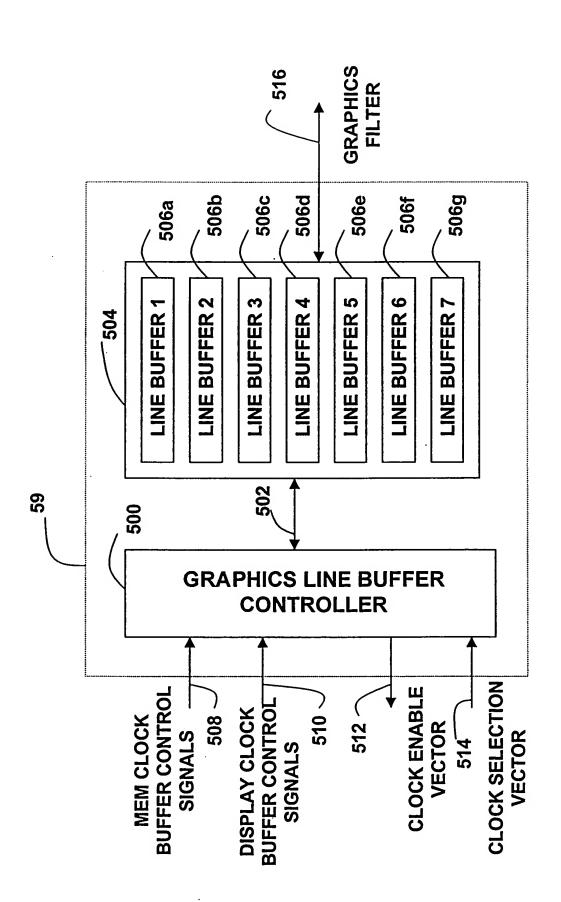Sheet 11 of 37

FIG. 11

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Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
Memory Architecture
Sheet 12 of 37

MEMORY CLOCK — 416

CLUT MEMORY REQUEST — 418

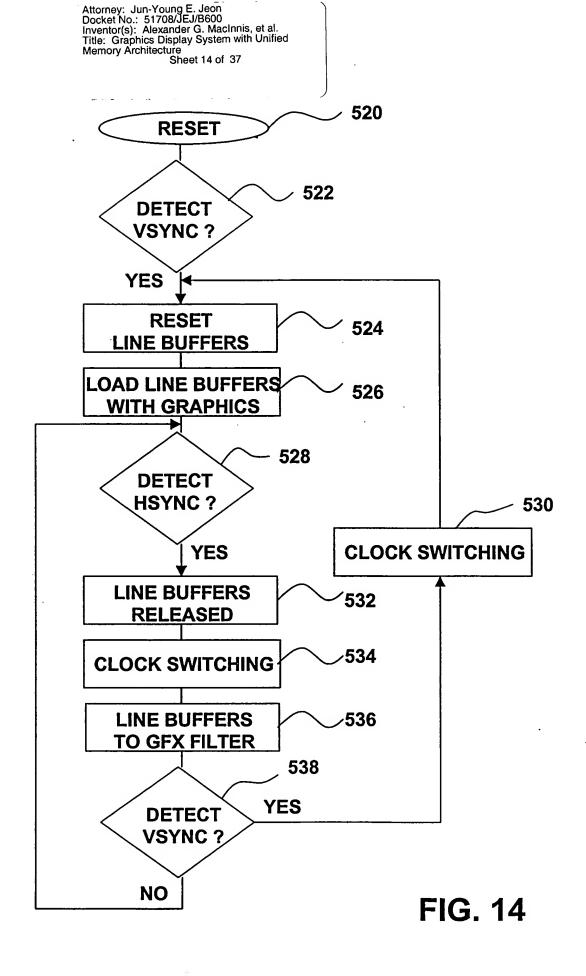CLUT MEMORY WRITE — 420
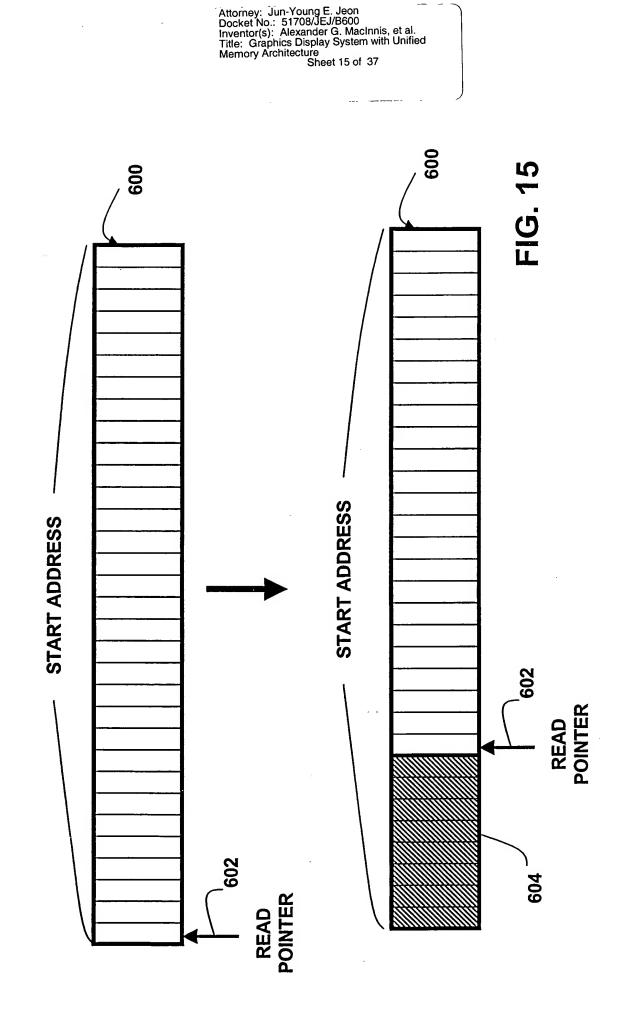
CLUT MEMORY DATA — 422

FIG. 12

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Docket No.: 51708/JEJ/B600
Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
Memory Architecture
Sheet 13 of 37

FIG. 13

GRAPHICS FILTER

516

506a

506b

506c

506d

506e

506f

506g

504

LINE BUFFER 1

LINE BUFFER 2

LINE BUFFER 3

LINE BUFFER 4

LINE BUFFER 5

LINE BUFFER 6

LINE BUFFER 7

59

500

502

GRAPHICS LINE BUFFER CONTROLLER

MEM CLOCK BUFFER CONTROL SIGNALS

508

DISPLAY CLOCK BUFFER CONTROL SIGNALS
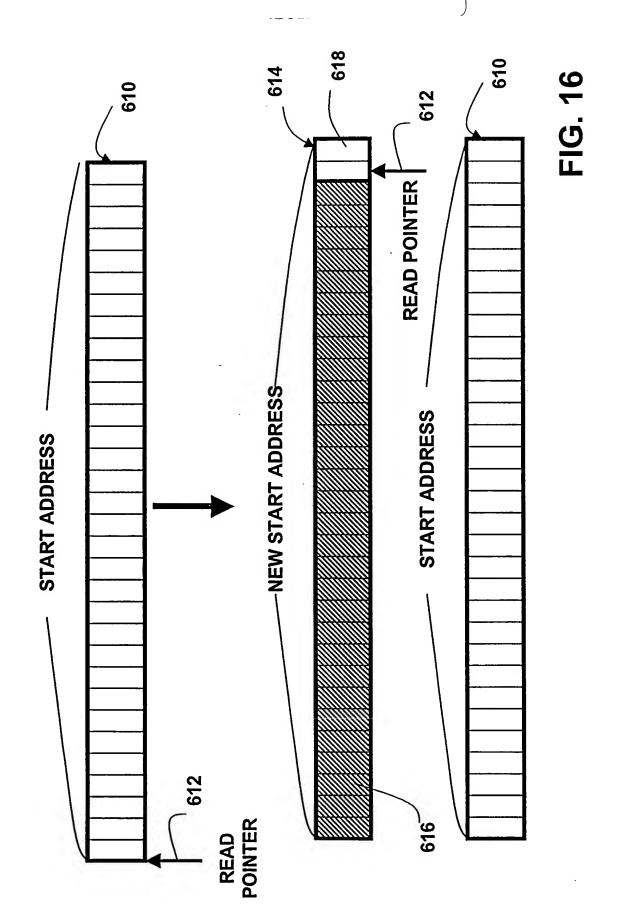
510

512

CLOCK ENABLE VECTOR

514

CLOCK SELECTION VECTOR

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Docket No.: 51708/JEJ/B600
Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
Memory Architecture
Sheet 14 of 37

RESET — 520

DETECT VSYNC ? — 522

YES

RESET LINE BUFFERS — 524

LOAD LINE BUFFERS WITH GRAPHICS — 526

DETECT HSYNC ? — 528

YES

CLOCK SWITCHING — 530

LINE BUFFERS RELEASED — 532

CLOCK SWITCHING — 534

LINE BUFFERS TO GFX FILTER — 536

DETECT VSYNC ? — 538

YES

NO

FIG. 14

Attorney: Jun-Young E. Jeon
Docket No.: 51708/JEJ/B600
Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
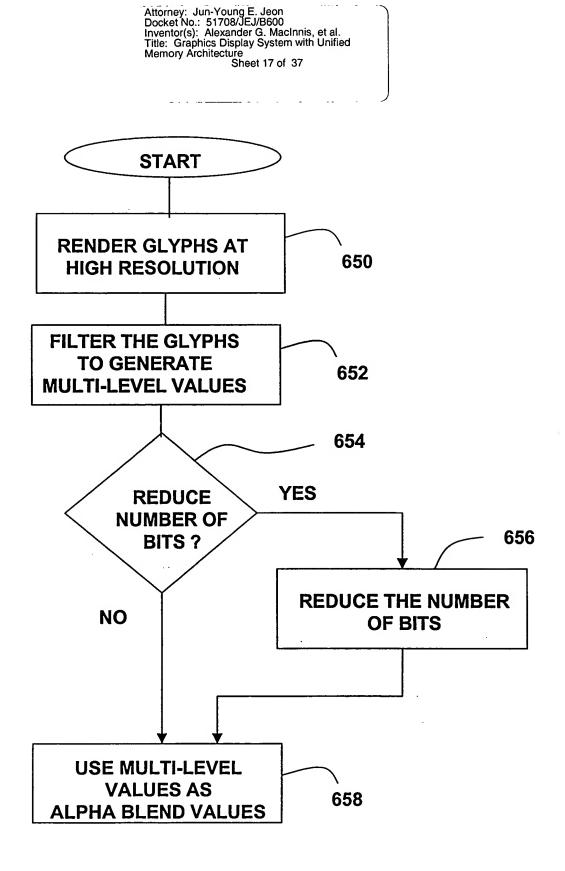Memory Architecture
Sheet 15 of 37

600

START ADDRESS

602

READ
POINTER

600

START ADDRESS

602

READ
POINTER

604

FIG. 15

Attorney: Jun-Young E. Jeon
Docket No.: 51708/JEJ/B600
Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
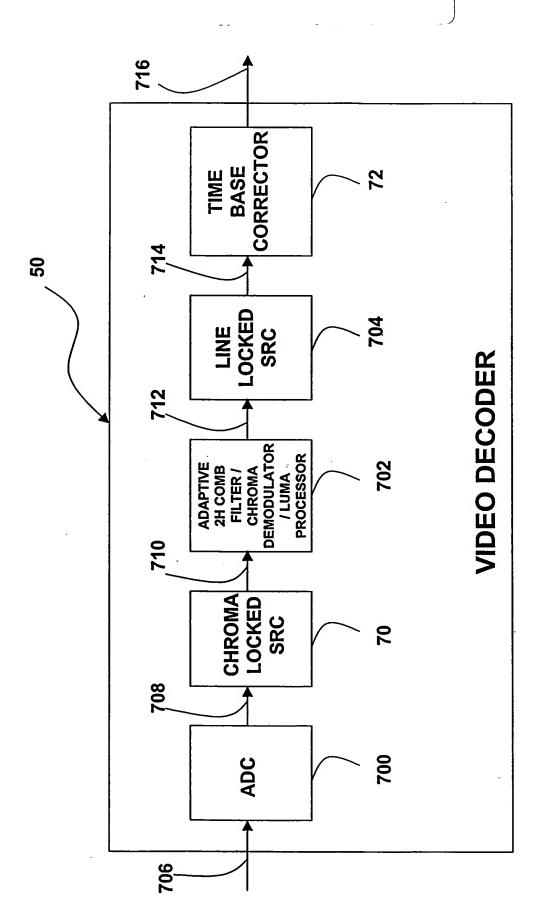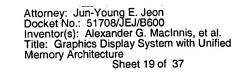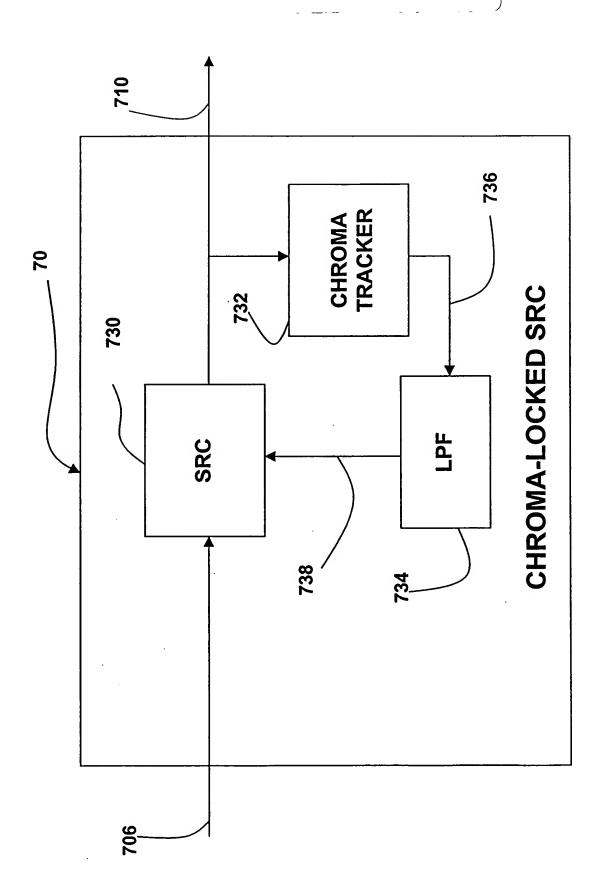Memory Architecture
Sheet 16 of 37

FIG. 16

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Docket No.: 51708/JEJ/B600
Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
Memory Architecture
Sheet 17 of 37

START

RENDER GLYPHS AT
HIGH RESOLUTION   650

FILTER THE GLYPHS
TO GENERATE
MULTI-LEVEL VALUES   652

654

REDUCE
NUMBER OF
BITS ?   YES

656

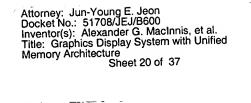NO   REDUCE THE NUMBER
OF BITS

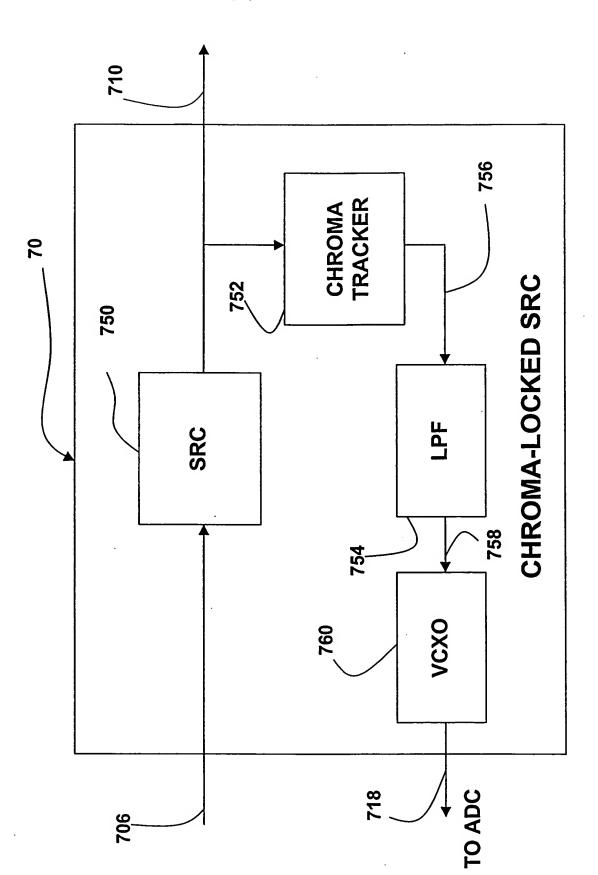USE MULTI-LEVEL
VALUES AS
ALPHA BLEND VALUES   658

FIG. 17

Attorney: Jun-Young E. Jeon
Docket No.: 51708/JEJ/B600
Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
Memory Architecture
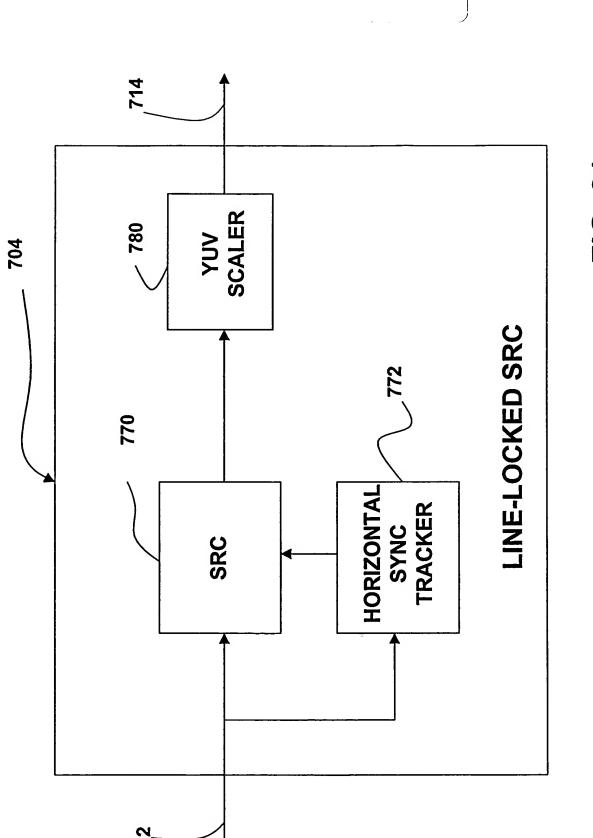   Sheet 18 of 37

VIDEO DECODER

FIG. 18

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Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
Memory Architecture
Sheet 19 of 37

710

70

706

730

SRC

732

CHROMA
TRACKER

736

738
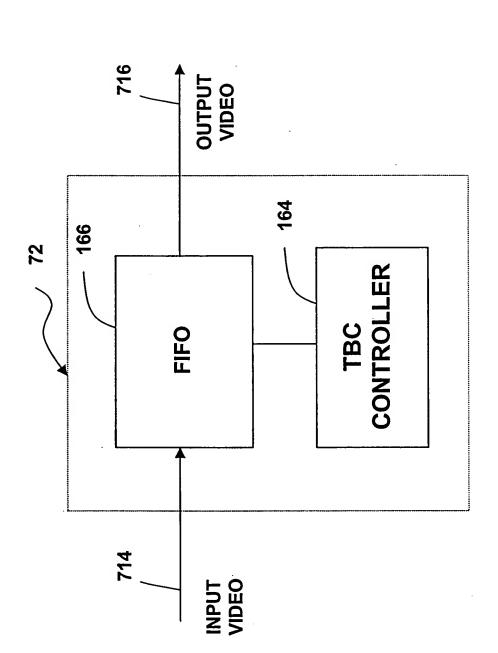
LPF

734

CHROMA-LOCKED SRC

FIG. 19

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Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
Memory Architecture
Sheet 20 of 37

FIG. 20

710

70

706

750

SRC

752

CHROMA
TRACKER

756

754

LPF

758

760

VCXO

718

TO ADC

CHROMA-LOCKED SRC

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Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
Memory Architecture
Sheet 21 of 37

714

704

780

YUV
SCALER

770

772

SRC

HORIZONTAL
SYNC
TRACKER

712

LINE-LOCKED SRC

FIG. 21

Attorney: Jun-Young E. Jeon
Docket No.: 51708/JEJ/B600
Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
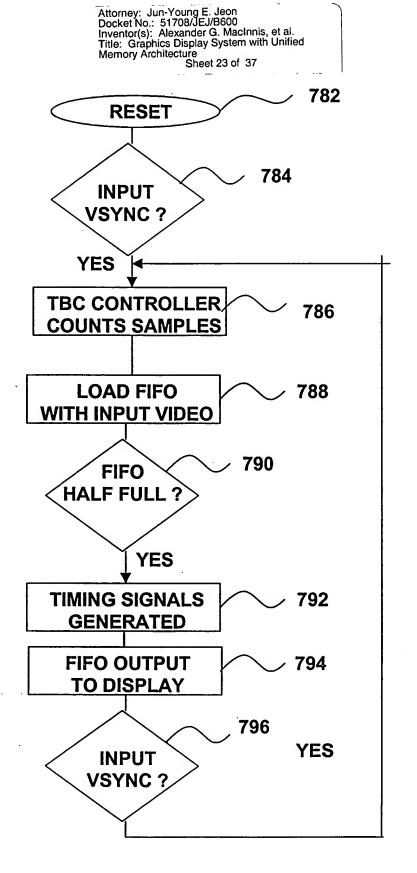Memory Architecture
Sheet 22 of 37

FIG. 22

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Docket No.: 51708/JEJ/B600
Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
Memory Architecture
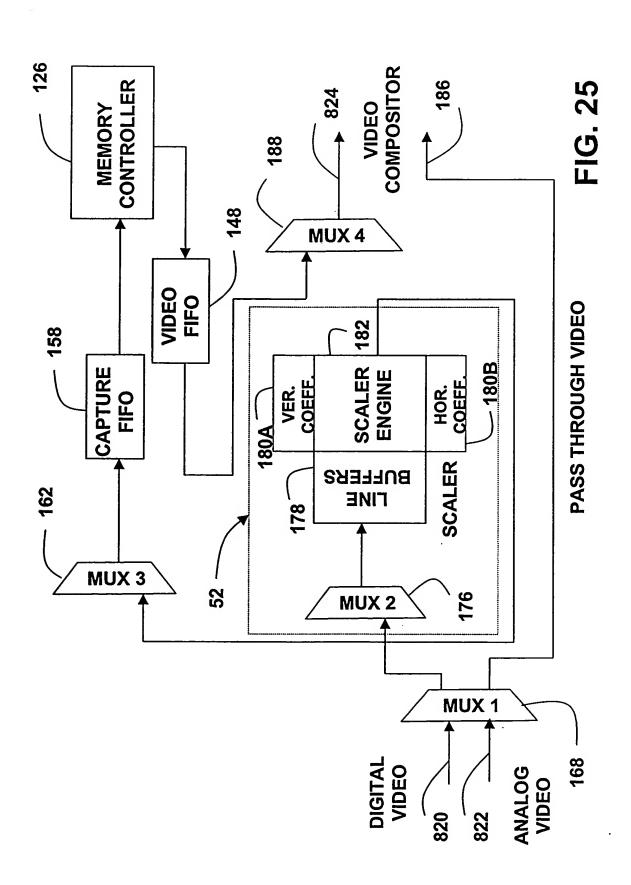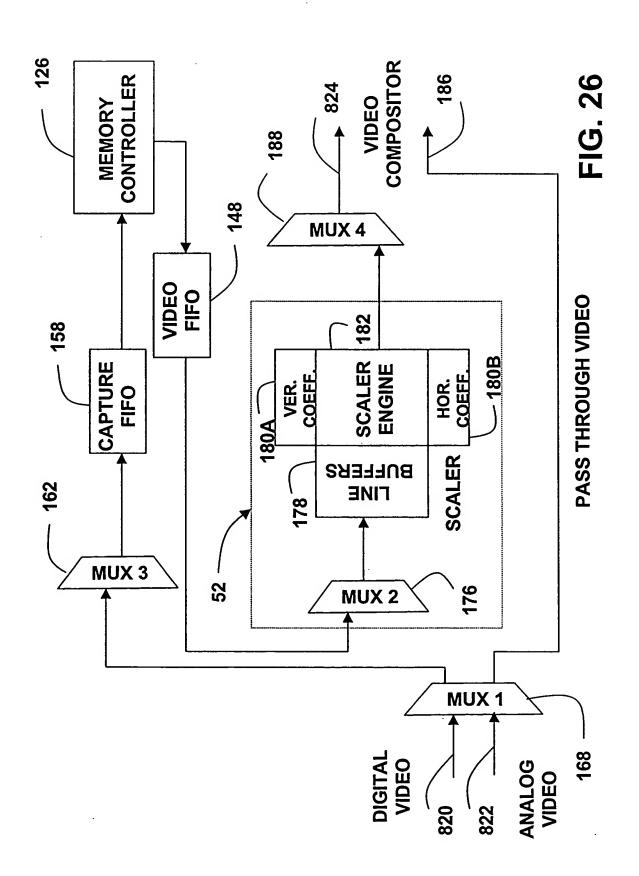Sheet 23 of 37

RESET — 782

INPUT VSYNC ? — 784

YES

TBC CONTROLLER COUNTS SAMPLES — 786

LOAD FIFO WITH INPUT VIDEO — 788

FIFO HALF FULL ? — 790

YES

TIMING SIGNALS GENERATED — 792

FIFO OUTPUT TO DISPLAY — 794

INPUT VSYNC ? — 796

YES

FIG. 23

INPUT

800

UP SCALE
OR
DOWN SCALE ?

802

DOWN SCALE

UP SCALE

SCALE
DOWN

804

806

CAPTURE IN
MEMORY

UP SCALE
OR
DOWN SCALE ?

808

DOWN SCALE

UP SCALE

SCALE
UP

812

810

814

OUTPUT

OUTPUT

FIG. 24

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Docket No.: 51708/JEJ/B600
Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
Memory Architecture
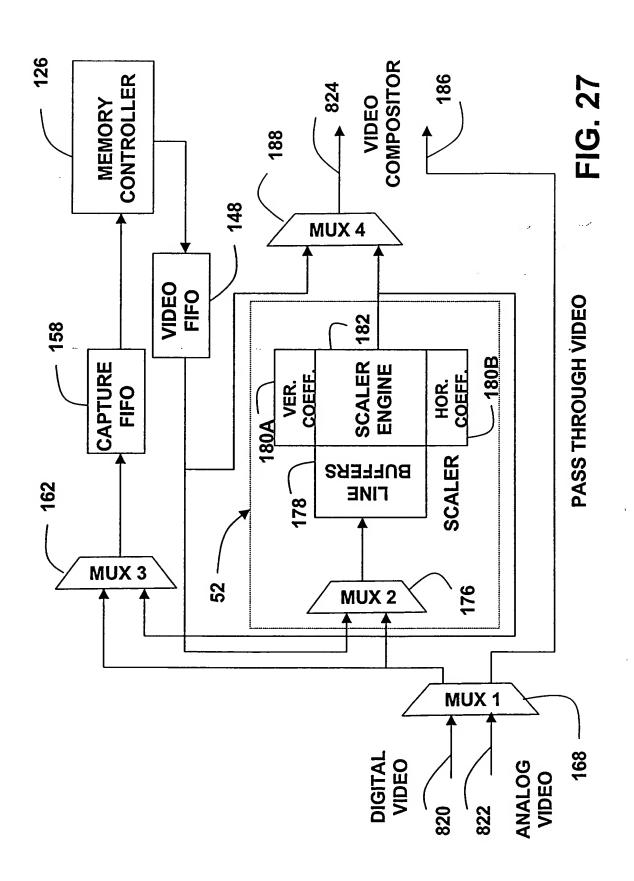Sheet 25 of 37

FIG. 25

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Docket No.: 51708/JEJ/B600
Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
Memory Architecture
Sheet 26 of 37

FIG. 26

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Docket No.: 51708/JEJ/B600
Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
Memory Architecture
Sheet 27 of 37

126 MEMORY CONTROLLER

148 VIDEO FIFO

158 CAPTURE FIFO

162 MUX 3

188 MUX 4

824 VIDEO COMPOSITOR

186

52

180A VER. COEFF.

182 SCALER ENGINE

180B HOR. COEFF.

178 LINE BUFFERS

SCALER

MUX 2 176

PASS THROUGH VIDEO

MUX 1

DIGITAL VIDEO

820

822

ANALOG VIDEO

168

FIG. 27

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Docket No.: 51708/JEJ/B600
Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
Memory Architecture
Sheet 28 of 37

RESET 902

BLEND GRAPHICS 904

FILTER
GRAPHICS WINDOW 906

BLEND
GRAPHICS WINDOW,
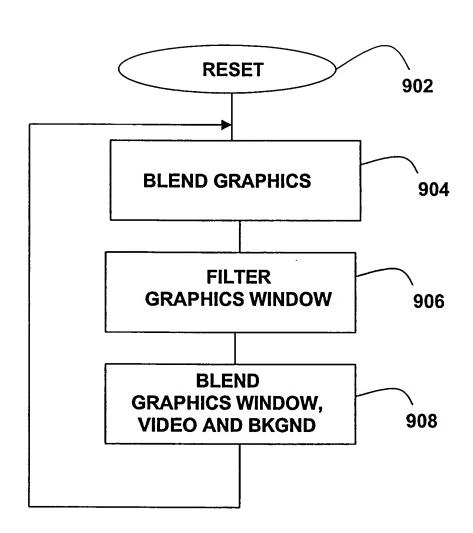VIDEO AND BKGND 908

FIG. 28

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Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
Memory Architecture
Sheet 29 of 37

RESET — 920

VSYNC ? — 922

LOAD BOTTOM MOST WINDOW — 924

BLEND NEXT WINDOW — 926

LAST WINDOW ON LINE — 928

NO

YES

LAST LINE OF FIELD ? — 930

NO

GO TO NEXT LINE — 932

YES

FIG. 29

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Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
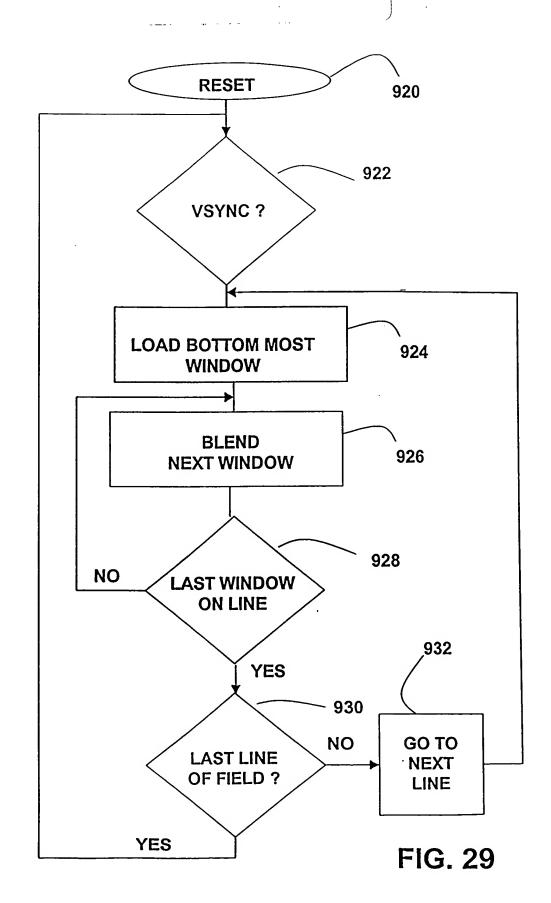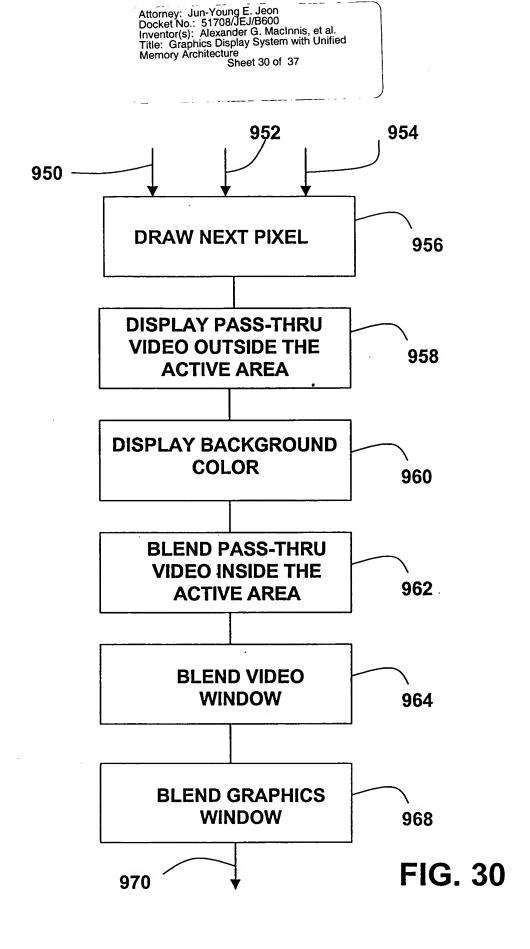Memory Architecture
Sheet 30 of 37

950   952   954

| DRAW NEXT PIXEL | 956 |

| DISPLAY PASS-THRU VIDEO OUTSIDE THE ACTIVE AREA | 958 |

| DISPLAY BACKGROUND COLOR | 960 |

| BLEND PASS-THRU VIDEO INSIDE THE ACTIVE AREA | 962 |

| BLEND VIDEO WINDOW | 964 |

| BLEND GRAPHICS WINDOW | 968 |

970

FIG. 30

Attorney: Jun-Young E. Jeon
Docket No.: 51708/JEJ/B600
Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
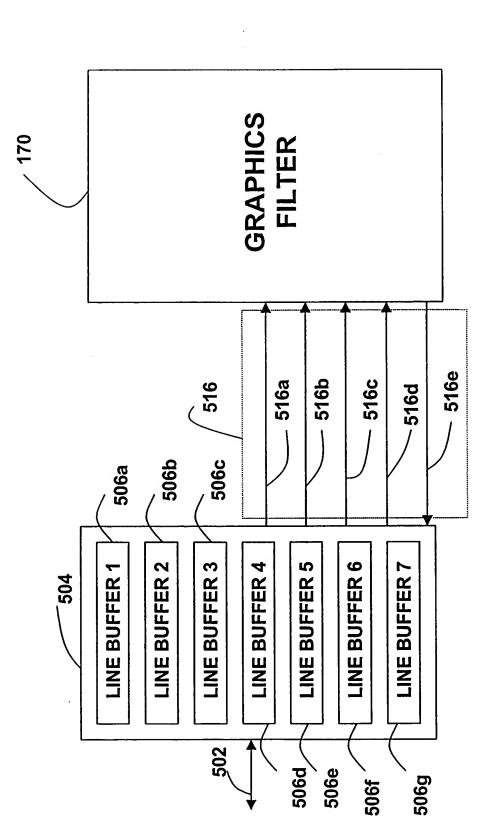Memory Architecture
Sheet 31 of 37

FIG. 31

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Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
Memory Architecture
Sheet 32 of 37

FIG.32

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Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
Memory Architecture
Sheet 33 of 37

FIG. 33

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Docket No.: 51708/JEJ/B600
Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
Memory Architecture
Sheet 34 of 37
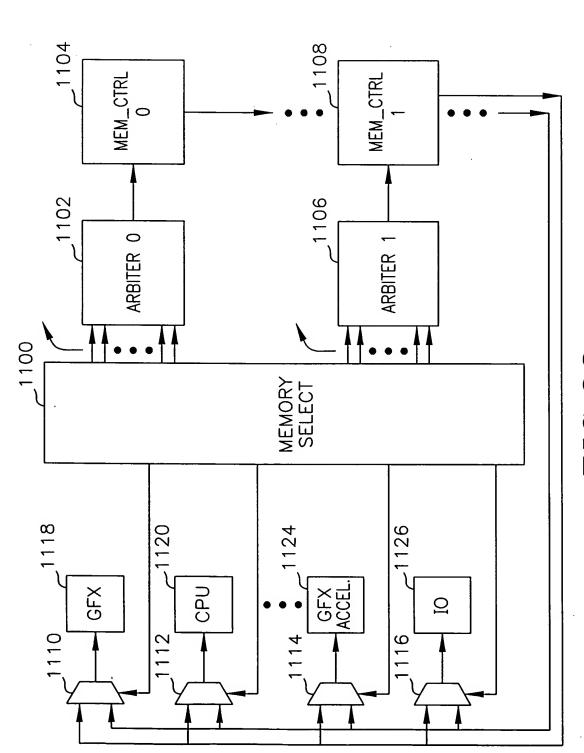
FIG. 34

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Docket No.: 51708/JEJ/B600
Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
Memory Architecture
Sheet 35 of 37
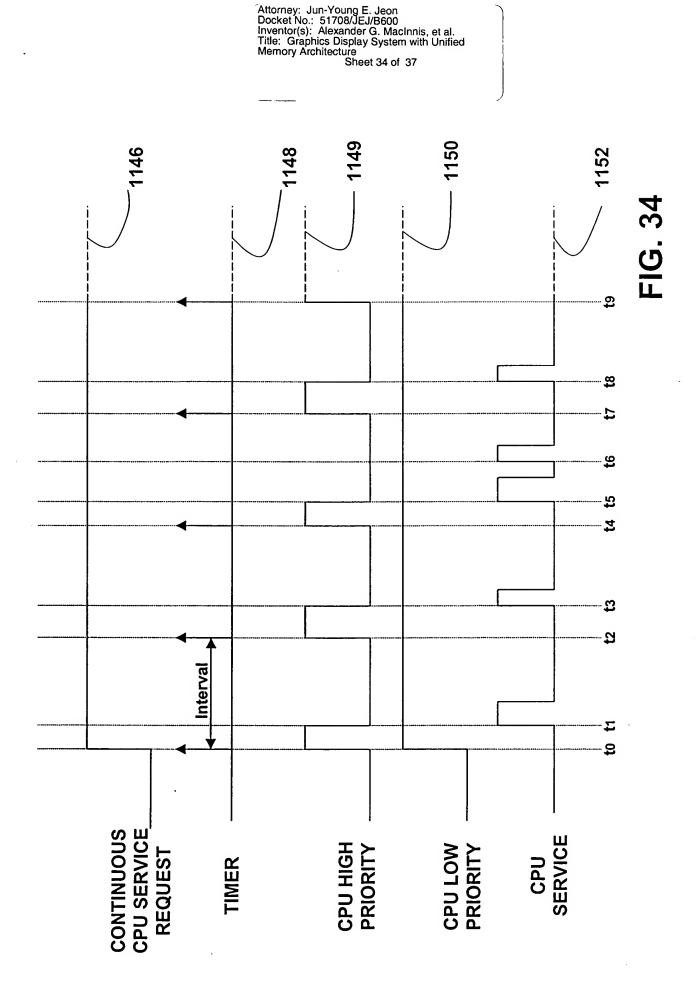
LOW PRIORITY
TASK

1154

TASK 1

1156

TASK 2

1158

TASK 3

1160

TASK 4

1162

t0 t1 t2 t3 t4 t5 t6 t7 t8 t9

FIG. 35

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Docket No.: 51708/JEJ/B600
Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
Memory Architecture
Sheet 36 of 37

HIGHEST PRIORITY

CPU READ REQUEST WITH BLOCKOUT COUNTER — 1170

GFX/WD READ REQUEST WITH BLOCKOUT COUNTER — 1172

ROUND ROBIN ARBITRATION FOR 2 CLIENTS

1174 — VIDEO WINDOW READ REQUEST

VIDEO CAPTURE WRITE REQUEST — 1176

REFRESH REQUEST — 1178

AUDIO READ REQUEST — 1180

ROUND ROBIN ARBITRATION FOR 5 CLIENTS

1182 — CPU READ REQUEST

GFX ACCELERATOR REQ. — 1184

1190 — CPU WRITE REQUEST

GFX/WD READ REQUEST — 1186

1188 — DMA READ/WRITE REQUEST

FIG.36

LOWEST PRIORITY

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Inventor(s): Alexander G. MacInnis, et al.
Title: Graphics Display System with Unified
Memory Architecture
Sheet 37 of 37

FIG. 37

MEMORY CONTROLLER 54

MEMORY 28

GRAPHICS ACCELERATOR 64

DMA 1304

QUEUE 1306

DATA SRAM 1302

VECTOR COPROCESSOR 1300

RESULT REGISTER 1310

INPUT REGISTER 1308

CPU 22